



H81H3-I

Rev : A

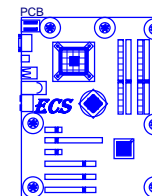
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REVISION HISTORY:

| Rev | Date | Notes |
|-----|------|------------------------|
| VA | | Modified from H81H3-M4 |


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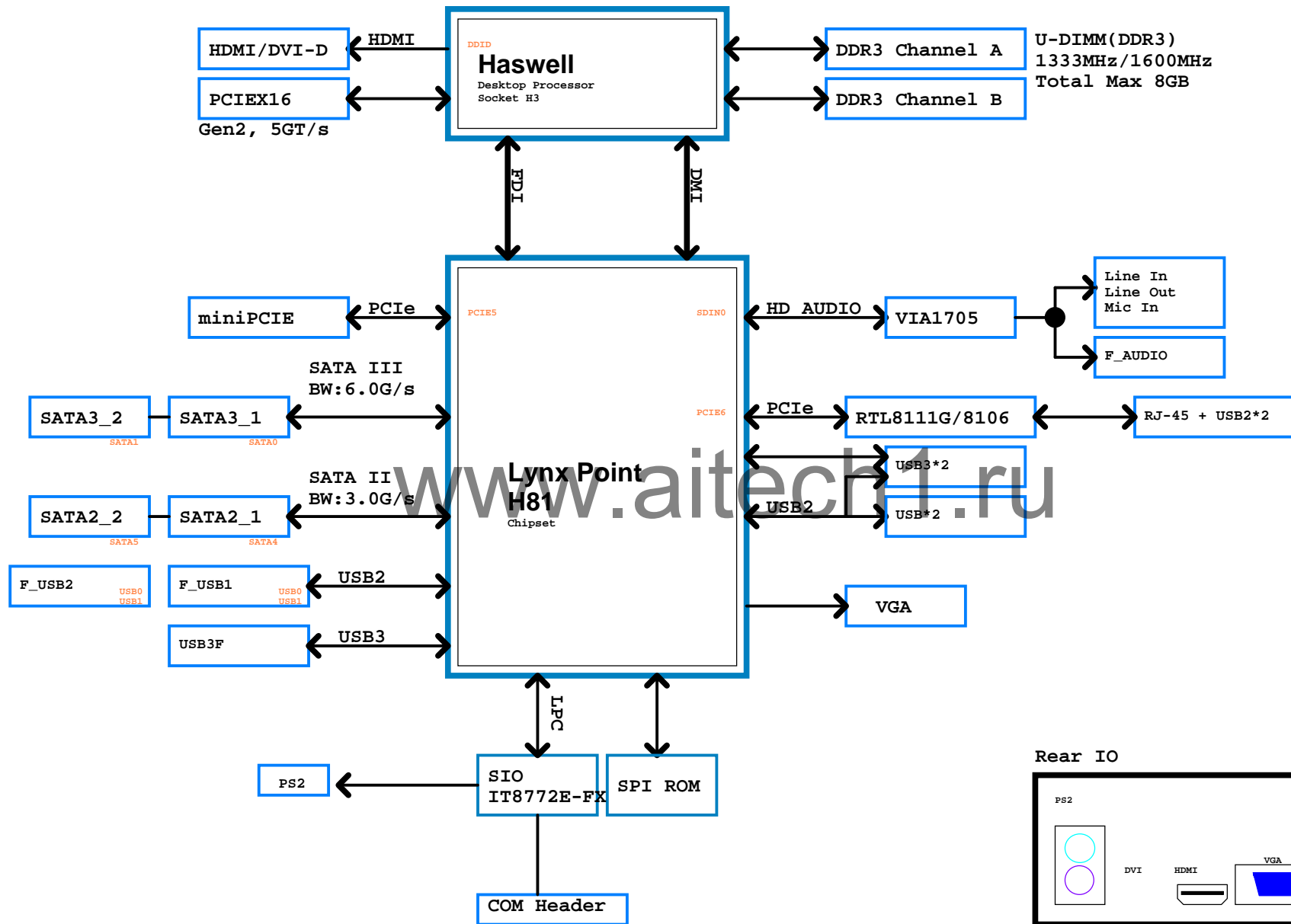


PCB : 170 x 170

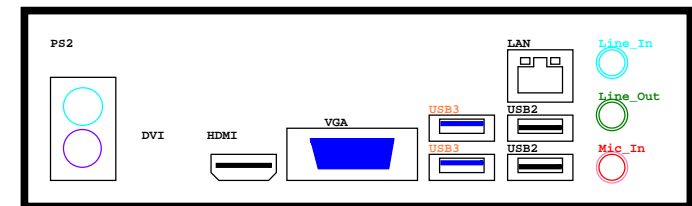
PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

- NOTE:**
1. Model Code:
 2. Modified from H81H3-M4

| | | |
|--|---------------------------------|----------|
|  Elitegroup Computer Systems | | |
| Title: Cover Page | | |
| Size: Custom | Document Number: H81H3-I | Rev: 1.0 |
| Date: Wednesday, August 14, 2013 | | |
| Sheet 1 of 27 | | |



Rear IO



Elitegroup Computer Systems

| | | | |
|--------|----------------------------|---------|---------------|
| Title | | | Block Diagram |
| Size | Document Number | H81H3-I | |
| Custom | | | Rev 1.0 |
| Date: | Wednesday, August 14, 2013 | Sheet | 2 of 27 |

PCH-GPIO function

| Pin Name | Power Well | Usage | Default Status |
|----------|------------|---------------------|-------------------------|
| GPIO0 | VCC3 | F_Audio Detection | GPI Hi : AC97 ; Lo: HD |
| GPIO1 | VCC3 | BOM Selection | GPI Hi : HDMI ; Lo: DVI |
| GPIO6 | VCC3 | BOM Selection | GPI |
| GPIO7 | VCC3 | BOM Selection | GPI |
| GPIO13 | 3VSB | LPC_PME | GPI |
| GPIO15 | | DIMM voltage adjust | Hi : 1.35V ; Lo: 1.5V |
| GPIO24 | | Me Unlock Control | |

SIO-GPIO function

| Pin Name | Power Well | Usage | Default Status |
|----------|------------|---------------|----------------|
| GP22 | 3VSB | G_LED1 | GPI |
| GP23 | 3VSB | G_LED2 | GPI |
| FAN_TAC2 | | CPU FAN Tac | |
| FAN_CTL2 | | CPU FAN Ctl | |
| VIN0 | | Vcore Voltage | |
| VIN1 | | Vdimm Voltage | |

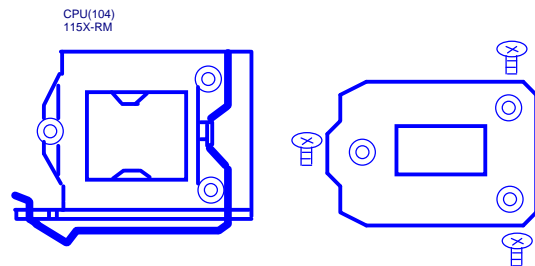
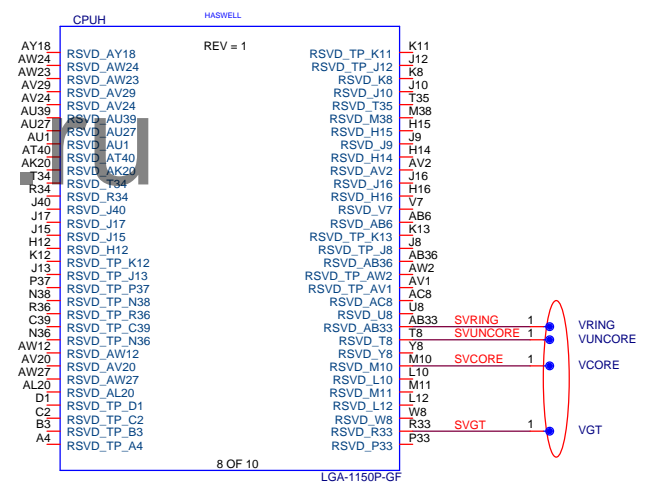
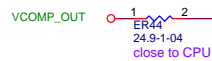
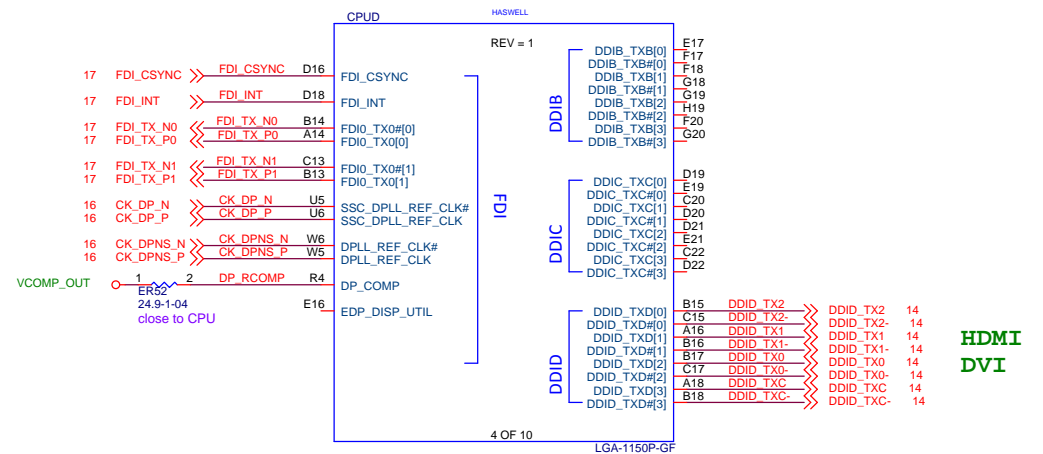
| | | | | |
|--------|----|----|----|-------|
| | S0 | S1 | S3 | S4/S5 |
| G_LED1 | H | H | L | L |
| G_LED2 | L | B | B | L |
| | G | GB | YB | OFF |

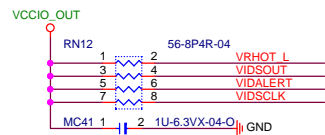
Blinking

Interrupt mapping

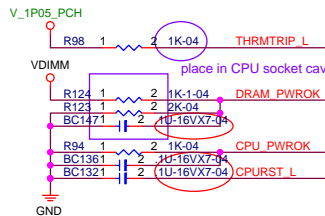
| Function | INT# port | PCle*1 port | Device |
|----------|-----------|-------------|---------------|
| PCIEX1 | INTD# | port 5 | LPT integrate |
| LAN | INTC# | port 6 | RTL8111G |
| SATA | INTB# | NA | LPT integrate |

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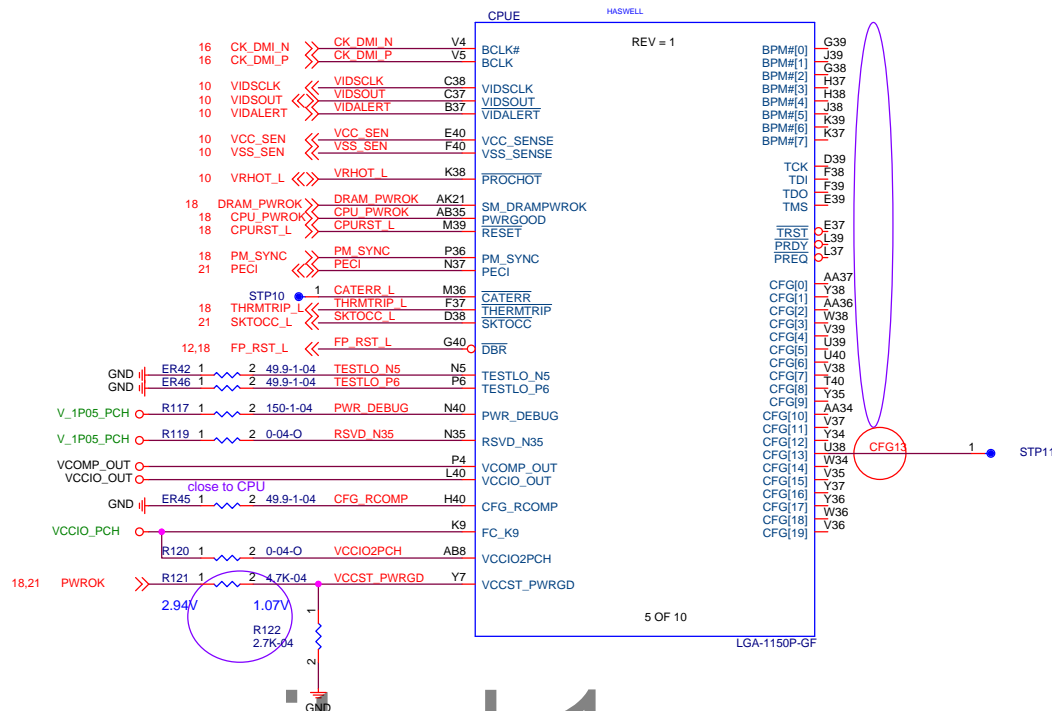
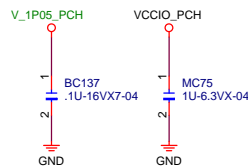




SPEC:
HOT: CPU 51,
SOUT: CPU 110, PWM 110,
ALERT: CPU 75,
CLK: PWM 55,



SPEC: 1V
Origin: Rt: 1.8K 5%, Rb: 3.3K 5%, 0.971V



CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
1 = Normal operation
0 = Lane numbers reversed.
CFG[3]: MSR Privacy Bit Feature
1 = Debug capability is determined by
IA32_Debug_Interface_MSR (0xC80) bit[0]
0 = IA32_Debug_Interface_MSR (0xC80) bit[0]
default setting overridden
CFG[5..6]: PCI Express* Bifurcation:
CFG[0..1, 4, 7..19]: Reserved configuration lane.

CFG[0..17] HAVE INTERNAL PULL-UPS

| PCIE CONFIG | CFG6 | CFG5 |
|-------------|------|------|
| 1 X 16 | 1 | 1 |
| 2 X 8 | 1 | 0 |
| Reserved | 0 | 1 |
| X6 X4 X4 | 0 | 0 |

External Connection

DDR3 CH.A

| | | |
|---|-----------------|-------------------|
| 8 | M_DATA_A[0..63] | ← M DATA A[0..63] |
| 8 | M_DQS_A_P[0..7] | ← M DQS A P[0..7] |
| 8 | M_DQS_A_N[0..7] | ← M DQS A N[0..7] |
| 8 | M_MA_A[0..15] | ← M MA A[0..15] |
| 8 | M_BS_A[0..2] | ← M BS A[0..2] |
| 8 | M_CS_A_L[2..3] | ← M CS A L[2..3] |
| 8 | M_CKE_A[2..3] | ← M CKE A[2..3] |
| 8 | M_ODT_A[2..3] | ← M ODT A[2..3] |
| 8 | M_CLK_A_P[2..3] | ← M CLK A P[2..3] |
| 8 | M_CLK_A_N[2..3] | ← M CLK A N[2..3] |
| 8 | DIMM_DQ_A | ← DIMM DQ_A |
| 8 | M_WE_A_L | ← M WE A_L |
| 8 | M_CAS_A_L | ← M CAS A_L |
| 8 | M_RAS_A_L | ← M RAS A_L |

DDR3 CH.B

| | | |
|-----|-----------------|-------------------|
| 9 | M_DATA_B[0..63] | ← M DATA B[0..63] |
| 9 | M_DQS_B_P[0..7] | ← M DQS B P[0..7] |
| 9 | M_DQS_B_N[0..7] | ← M DQS B N[0..7] |
| 9 | M_MA_B[0..15] | ← M MA B[0..15] |
| 9 | M_BS_B[0..2] | ← M BS B[0..2] |
| 9 | M_CS_B_L[2..3] | ← M CS B L[2..3] |
| 9 | M_CKE_B[2..3] | ← M CKE B[2..3] |
| 9 | M_ODT_B[2..3] | ← M ODT B[2..3] |
| 9 | M_CLK_B_P[2..3] | ← M CLK B P[2..3] |
| 9 | M_CLK_B_N[2..3] | ← M CLK B N[2..3] |
| 9 | DIMM_DQ_B | ← DIMM DQ_B |
| 9 | M_WE_B_L | ← M WE B_L |
| 9 | M_CAS_B_L | ← M CAS B_L |
| 9 | M_RAS_B_L | ← M RAS B_L |
| 8,9 | DRAMRST_L | ← DRAMRST_L |
| 8,9 | DIMM_CA | ← DIMM CA |

**Attention

| CPUA | | HASWELL | |
|-------------|------|------------|-----------|
| REV = 1 | | | |
| M DATA A0 | AD38 | SA_DQ[0] | SA_MA[0] |
| M DATA A1 | AD39 | SA_DQ[1] | SA_MA[1] |
| M DATA A2 | AF38 | SA_DQ[2] | SA_MA[2] |
| M DATA A3 | AF39 | SA_DQ[3] | SA_MA[3] |
| M DATA A4 | AD37 | SA_DQ[4] | SA_MA[4] |
| M DATA A5 | AD40 | SA_DQ[5] | SA_MA[5] |
| M DATA A6 | AF37 | SA_DQ[6] | SA_MA[6] |
| M DATA A7 | AF40 | SA_DQ[7] | SA_MA[7] |
| M DATA A8 | AH40 | SA_DQ[8] | SA_MA[8] |
| M DATA A9 | AH39 | SA_DQ[9] | SA_MA[9] |
| M DATA A10 | AK38 | SA_DQ[10] | SA_MA[10] |
| M DATA A11 | AK39 | SA_DQ[11] | SA_MA[11] |
| M DATA A12 | AH37 | SA_DQ[12] | SA_MA[12] |
| M DATA A13 | AH38 | SA_DQ[13] | SA_MA[13] |
| M DATA A14 | AK37 | SA_DQ[14] | SA_MA[14] |
| M DATA A15 | AK40 | SA_DQ[15] | SA_MA[15] |
| M DATA A16 | AM40 | SA_DQ[16] | SA_MA[16] |
| M DATA A17 | AM39 | SA_DQ[17] | SA_ODT[0] |
| M DATA A18 | AP38 | SA_DQ[18] | SA_ODT[1] |
| M DATA A19 | AP39 | SA_DQ[19] | SA_ODT[2] |
| M DATA A20 | AM37 | SA_DQ[20] | SA_ODT[3] |
| M DATA A21 | AM38 | SA_DQ[21] | SA_ODT[0] |
| M DATA A22 | AP37 | SA_DQ[22] | SA_ODT[1] |
| M DATA A23 | AP40 | SA_DQ[23] | SA_ODT[2] |
| M DATA A24 | AV39 | SA_DQ[24] | SA_ODT[3] |
| M DATA A25 | AW37 | SA_DQ[25] | SA_ODT[0] |
| M DATA A26 | AU35 | SA_DQ[26] | SA_ODT[1] |
| M DATA A27 | AV35 | SA_DQ[27] | SA_ODT[2] |
| M DATA A28 | AT37 | SA_DQ[28] | SA_ODT[3] |
| M DATA A29 | AU37 | SA_DQ[29] | SA_ODT[0] |
| M DATA A30 | AT35 | SA_DQ[30] | SA_ODT[1] |
| M DATA A31 | AV35 | SA_DQ[31] | SA_ODT[2] |
| M DATA A32 | AY6 | SA_DQ[32] | SA_ODT[3] |
| M DATA A33 | AU6 | SA_DQ[33] | SA_ODT[0] |
| M DATA A34 | AV4 | SA_DQ[34] | SA_ODT[1] |
| M DATA A35 | AU4 | SA_DQ[35] | SA_ODT[2] |
| M DATA A36 | AW6 | SA_DQ[36] | SA_ODT[3] |
| M DATA A37 | AV6 | SA_DQ[37] | SA_ODT[0] |
| M DATA A38 | AW4 | SA_DQ[38] | SA_ODT[1] |
| M DATA A39 | AY4 | SA_DQ[39] | SA_ODT[2] |
| M DATA A40 | AR1 | SA_DQ[40] | SA_ODT[3] |
| M DATA A41 | AR4 | SA_DQ[41] | SA_ODT[0] |
| M DATA A42 | AN3 | SA_DQ[42] | SA_ODT[1] |
| M DATA A43 | AN4 | SA_DQ[43] | SA_ODT[2] |
| M DATA A44 | AR2 | SA_DQ[44] | SA_ODT[3] |
| M DATA A45 | AR3 | SA_DQ[45] | SA_ODT[0] |
| M DATA A46 | AN2 | SA_DQ[46] | SA_ODT[1] |
| M DATA A47 | AN1 | SA_DQ[47] | SA_ODT[2] |
| M DATA A48 | AL1 | SA_DQ[48] | SA_ODT[3] |
| M DATA A49 | AL2 | SA_DQ[49] | SA_ODT[0] |
| M DATA A50 | AJ3 | SA_DQ[50] | SA_ODT[1] |
| M DATA A51 | AJ4 | SA_DQ[51] | SA_ODT[2] |
| M DATA A52 | AL2 | SA_DQ[52] | SA_ODT[3] |
| M DATA A53 | AJ2 | SA_DQ[53] | SA_ODT[0] |
| M DATA A54 | AJ1 | SA_DQ[54] | SA_ODT[1] |
| M DATA A55 | AG1 | SA_DQ[55] | SA_ODT[2] |
| M DATA A56 | AG4 | SA_DQ[56] | SA_ODT[3] |
| M DATA A57 | AE3 | SA_DQ[57] | SA_ODT[0] |
| M DATA A58 | AE4 | SA_DQ[58] | SA_ODT[1] |
| M DATA A59 | AG2 | SA_DQ[59] | SA_ODT[2] |
| M DATA A60 | AG3 | SA_DQ[60] | SA_ODT[3] |
| M DATA A61 | AE2 | SA_DQ[61] | SA_ODT[0] |
| M DATA A62 | AE1 | SA_DQ[62] | SA_ODT[1] |
| M DATA A63 | AE39 | SA_DQ[63] | SA_ODT[2] |
| M DQS A P0 | AE39 | SA_DQS[0] | SA_ODT[3] |
| M DQS A P1 | AJ39 | SA_DQS[1] | SA_ODT[0] |
| M DQS A P2 | AN39 | SA_DQS[2] | SA_ODT[1] |
| M DQS A P3 | AV36 | SA_DQS[3] | SA_ODT[2] |
| M DQS A P4 | AV5 | SA_DQS[4] | SA_ODT[3] |
| M DQS A P5 | AP3 | SA_DQS[5] | SA_ODT[0] |
| M DQS A P6 | AK3 | SA_DQS[6] | SA_ODT[1] |
| M DQS A P7 | AF3 | SA_DQS[7] | SA_ODT[2] |
| M DQS A N0 | AE38 | SA_DQS[8] | SA_ODT[3] |
| M DQS A N1 | AJ38 | SA_DQS[9] | SA_ODT[0] |
| M DQS A N2 | AN38 | SA_DQS[10] | SA_ODT[1] |
| M DQS A N3 | AJ36 | SA_DQS[11] | SA_ODT[2] |
| M DQS A N4 | AW5 | SA_DQS[12] | SA_ODT[3] |
| M DQS A N5 | AP2 | SA_DQS[13] | SA_ODT[0] |
| M DQS A N6 | AK2 | SA_DQS[14] | SA_ODT[1] |
| M DQS A N7 | AF2 | SA_DQS[15] | SA_ODT[2] |
| M DQS A N8 | AF2 | SA_DQS[16] | SA_ODT[3] |
| M DQS A N9 | AJ32 | SA_DQS[17] | SA_ODT[0] |
| M DQS A N10 | AJ32 | SA_DQS[18] | SA_ODT[1] |

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**Attention

| CPUB | | HASWELL | |
|------------|------|------------|-----------|
| REV = 1 | | | |
| M DATA B0 | AE34 | SB_DQ[0] | SB_MA[0] |
| M DATA B1 | AE35 | SB_DQ[1] | SB_MA[1] |
| M DATA B2 | AG35 | SB_DQ[2] | SB_MA[2] |
| M DATA B3 | AH35 | SB_DQ[3] | SB_MA[3] |
| M DATA B4 | AD34 | SB_DQ[4] | SB_MA[4] |
| M DATA B5 | AD35 | SB_DQ[5] | SB_MA[5] |
| M DATA B6 | AG34 | SB_DQ[6] | SB_MA[6] |
| M DATA B7 | AH34 | SB_DQ[7] | SB_MA[7] |
| M DATA B8 | AL34 | SB_DQ[8] | SB_MA[8] |
| M DATA B9 | AL35 | SB_DQ[9] | SB_MA[9] |
| M DATA B10 | AK31 | SB_DQ[10] | SB_MA[10] |
| M DATA B11 | AL31 | SB_DQ[11] | SB_MA[11] |
| M DATA B12 | AK34 | SB_DQ[12] | SB_MA[12] |
| M DATA B13 | AK35 | SB_DQ[13] | SB_MA[13] |
| M DATA B14 | AK32 | SB_DQ[14] | SB_MA[14] |
| M DATA B15 | AL32 | SB_DQ[15] | SB_MA[15] |
| M DATA B16 | AN34 | SB_DQ[16] | SB_ODT[0] |
| M DATA B17 | AP34 | SB_DQ[17] | SB_ODT[1] |
| M DATA B18 | AP31 | SB_DQ[18] | SB_ODT[2] |
| M DATA B19 | AN35 | SB_DQ[19] | SB_ODT[3] |
| M DATA B20 | AP35 | SB_DQ[20] | SB_ODT[0] |
| M DATA B21 | AN32 | SB_DQ[21] | SB_ODT[1] |
| M DATA B22 | AP32 | SB_DQ[22] | SB_ODT[2] |
| M DATA B23 | AP32 | SB_DQ[23] | SB_ODT[3] |
| M DATA B24 | AM28 | SB_DQ[24] | SB_ODT[0] |
| M DATA B25 | AR29 | SB_DQ[25] | SB_ODT[1] |
| M DATA B26 | AR28 | SB_DQ[26] | SB_ODT[2] |
| M DATA B27 | AL29 | SB_DQ[27] | SB_ODT[3] |
| M DATA B28 | AL28 | SB_DQ[28] | SB_ODT[0] |
| M DATA B29 | AP29 | SB_DQ[29] | SB_ODT[1] |
| M DATA B30 | AP28 | SB_DQ[30] | SB_ODT[2] |
| M DATA B31 | AR12 | SB_DQ[31] | SB_ODT[3] |
| M DATA B32 | AP12 | SB_DQ[32] | SB_ODT[0] |
| M DATA B33 | AP12 | SB_DQ[33] | SB_ODT[1] |
| M DATA B34 | AL13 | SB_DQ[34] | SB_ODT[2] |
| M DATA B35 | AR13 | SB_DQ[35] | SB_ODT[3] |
| M DATA B36 | AP13 | SB_DQ[36] | SB_ODT[0] |
| M DATA B37 | AM13 | SB_DQ[37] | SB_ODT[1] |
| M DATA B38 | AM12 | SB_DQ[38] | SB_ODT[2] |
| M DATA B39 | AM12 | SB_DQ[39] | SB_ODT[3] |
| M DATA B40 | AR9 | SB_DQ[40] | SB_ODT[0] |
| M DATA B41 | AR9 | SB_DQ[41] | SB_ODT[1] |
| M DATA B42 | AR6 | SB_DQ[42] | SB_ODT[2] |
| M DATA B43 | AP6 | SB_DQ[43] | SB_ODT[3] |
| M DATA B44 | AR10 | SB_DQ[44] | SB_ODT[0] |
| M DATA B45 | AP10 | SB_DQ[45] | SB_ODT[1] |
| M DATA B46 | AR7 | SB_DQ[46] | SB_ODT[2] |
| M DATA B47 | AR7 | SB_DQ[47] | SB_ODT[3] |
| M DATA B48 | AM9 | SB_DQ[48] | SB_ODT[0] |
| M DATA B49 | AL9 | SB_DQ[49] | SB_ODT[1] |
| M DATA B50 | AL6 | SB_DQ[50] | SB_ODT[2] |
| M DATA B51 | AL7 | SB_DQ[51] | SB_ODT[3] |
| M DATA B52 | AM10 | SB_DQ[52] | SB_ODT[0] |
| M DATA B53 | AM6 | SB_DQ[53] | SB_ODT[1] |
| M DATA B54 | AM7 | SB_DQ[54] | SB_ODT[2] |
| M DATA B55 | AH6 | SB_DQ[55] | SB_ODT[3] |
| M DATA B56 | AH7 | SB_DQ[56] | SB_ODT[0] |
| M DATA B57 | AE7 | SB_DQ[57] | SB_ODT[1] |
| M DATA B58 | AJ6 | SB_DQ[58] | SB_ODT[2] |
| M DATA B59 | AJ7 | SB_DQ[59] | SB_ODT[3] |
| M DATA B60 | AJ7 | SB_DQ[60] | SB_ODT[0] |
| M DATA B61 | AF7 | SB_DQ[61] | SB_ODT[1] |
| M DQS B P0 | AP35 | SB_DQS[0] | SB_ODT[2] |
| M DQS B P1 | AL33 | SB_DQS[1] | SB_ODT[3] |
| M DQS B P2 | AP33 | SB_DQS[2] | SB_ODT[0] |
| M DQS B P3 | AN28 | SB_DQS[3] | SB_ODT[1] |
| M DQS B P4 | AN12 | SB_DQS[4] | SB_ODT[2] |
| M DQS B P5 | AP8 | SB_DQS[5] | SB_ODT[3] |
| M DQS B P6 | AL8 | SB_DQS[6] | SB_ODT[0] |
| M DQS B P7 | AG7 | SB_DQS[7] | SB_ODT[1] |
| M DQS B N0 | AN25 | SB_DQS[8] | SB_ODT[2] |
| M DQS B N1 | AF34 | SB_DQS[9] | SB_ODT[3] |
| M DQS B N2 | AK33 | SB_DQS[10] | SB_ODT[0] |
| M DQS B N3 | AN33 | SB_DQS[11] | SB_ODT[1] |
| M DQS B N4 | AN29 | SB_DQS[12] | SB_ODT[2] |
| M DQS B N5 | AN13 | SB_DQS[13] | SB_ODT[3] |
| M DQS B N6 | AR8 | SB_DQS[14] | SB_ODT[0] |
| M DQS B N7 | AM8 | SB_DQS[15] | SB_ODT[1] |
| M DQS B N8 | AG6 | SB_DQS[16] | SB_ODT[2] |
| M DQS B N9 | AN28 | SB_DQS[17] | SB_ODT[3] |

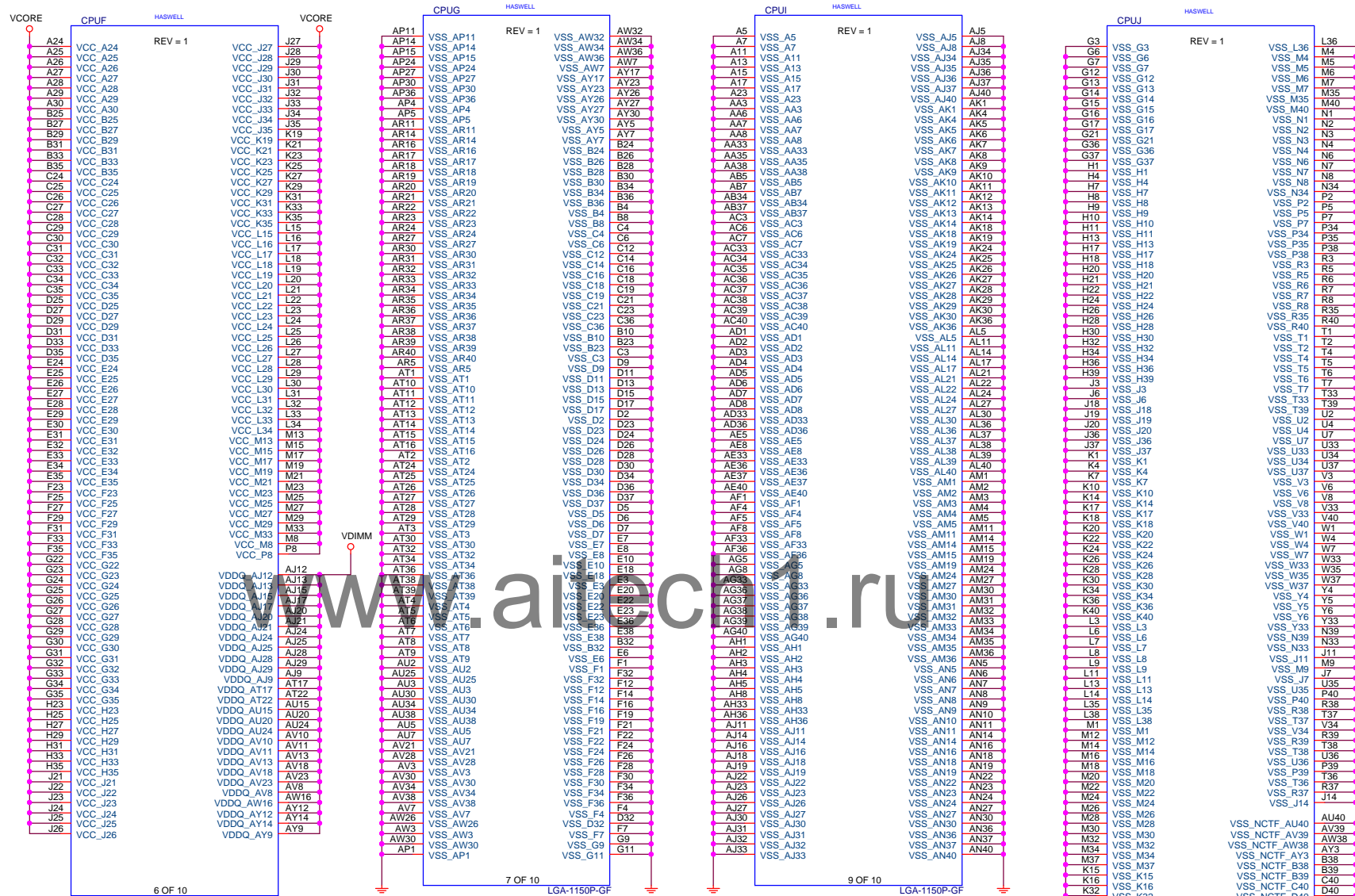
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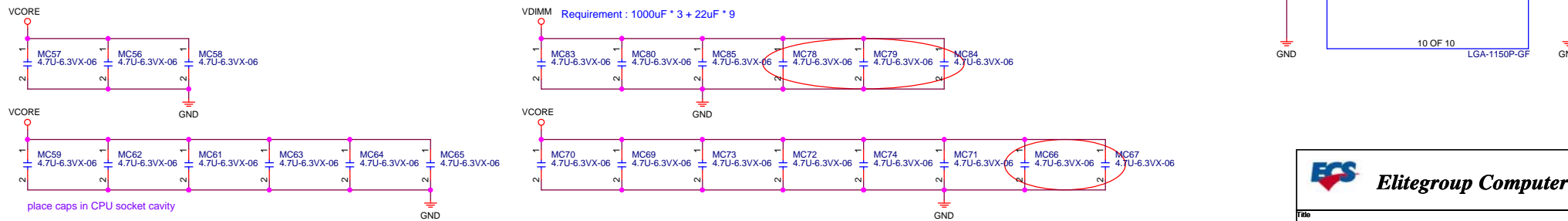
Elitegroup Computer Systems

| | | | |
|--------|----------------------------|----------|---------|
| Title | | CPU-DDR3 | |
| Size | Document Number | H81H3-I | |
| Custom | | Rev 1.0 | |
| Date: | Wednesday, August 14, 2013 | Sheet | 6 of 27 |




Requirement : 470uF * 5 (+3 no-stuff) + 22uF * 22

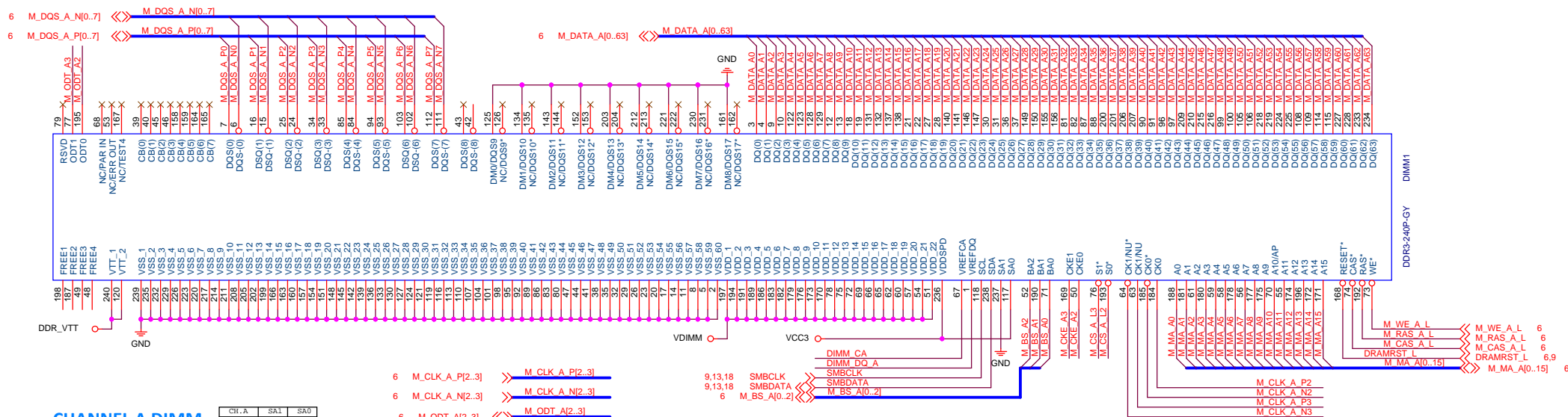
Requirement : 1000uF * 3 + 22uF * 9



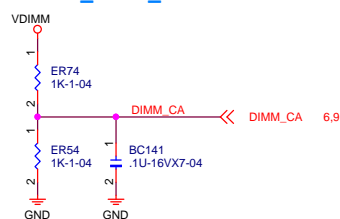
place caps in CPU socket cavity

**Elitegroup Computer Systems**

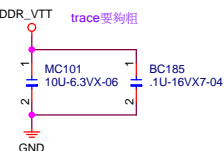
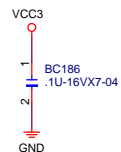
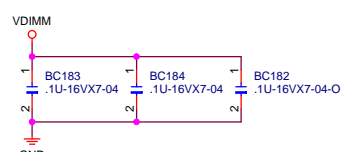
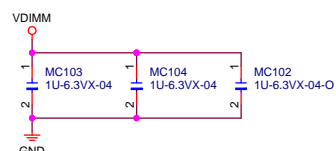
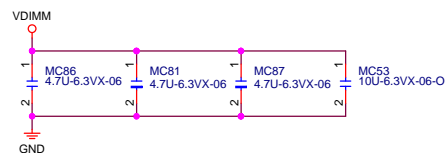
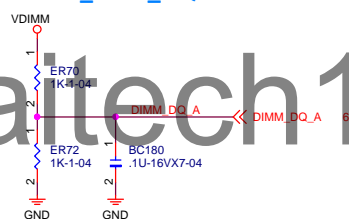
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| Title | | | CPU-PWR/GND | | |
| Size | Document Number | | H81H3-I | | Rev |
| Custom | | | | | 1.0 |
| Date: | Wednesday, August 14, 2013 | | Sheet | 7 | of 27 |



DIMM_VREF_CA Circuit

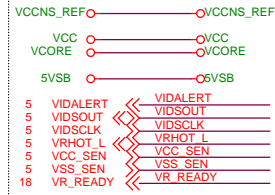


DIMM_VREF_DQ Circuit



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External Connection



SET1:

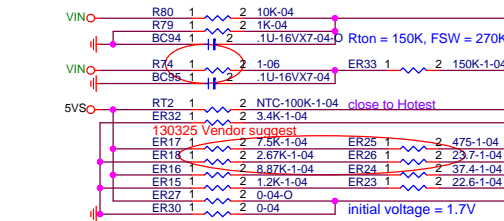
Rt1 = 7.5K+475, Rb1 = 2.67K+23.7,
Ramp (RSET % 130K Rton) = 87.5%, DVID_Width = 192us,
OCP = 150% ICCMAX, DVID_Threshold = 15mV,

SET2:

Ri2 = 8.87K+37.4, Rb2 = 1.2K+22.6,
QR Threshold = disable, QR Width = 111%,
ICCMAX = 96A,

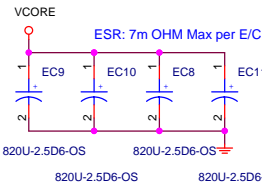
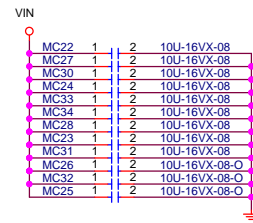
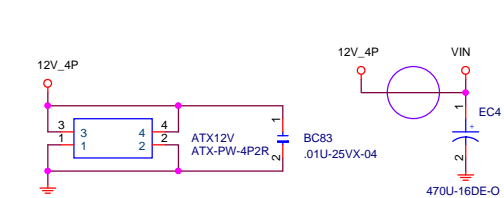
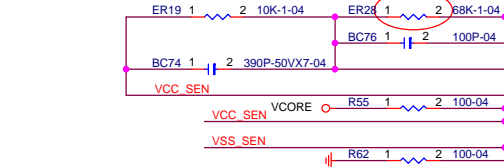
SET3: Rb3 = 0ohm,
Offset = 1/2*(Ri3/Rb3 - 1.2) = 0mV,

When 100度 NTC-100K min value : 5.09K,
Visen = 5 * 3.45 / (5.09+3.45) = 1.880 < 1.886,

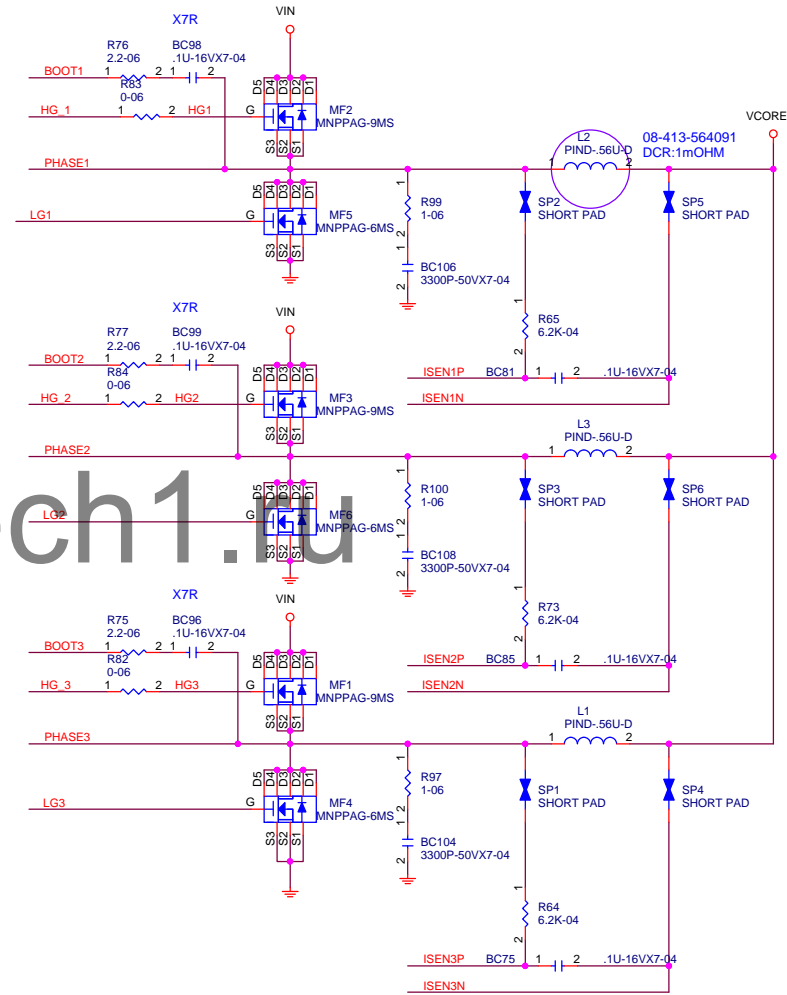


Req = (NTC-100K + 16.5K) // 11K + 2K = 12.05K

130325 Vendor suggest 68K for load line. origin 60.4K

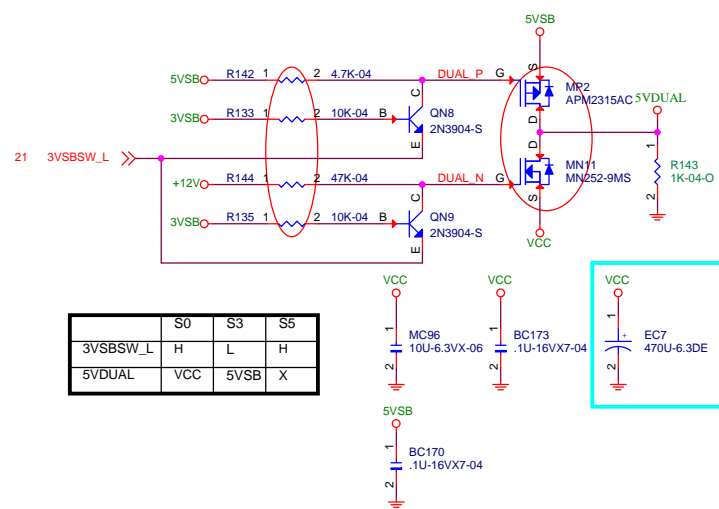


Power Down Sequencing Circuit



2 phase option



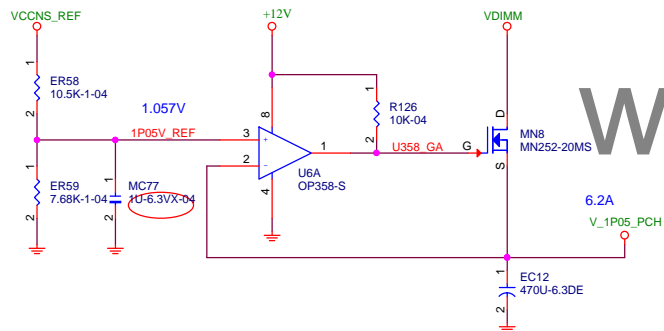


| | S0 | S3 | S5 |
|---------|-----|------|----|
| 3VBSW_L | H | L | H |
| 5VDUAL | VCC | 5VSB | X |

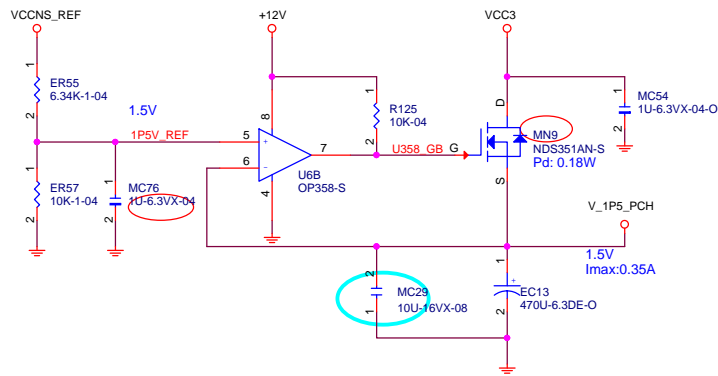
$$R_{ocset} = I_{oc} * R_{ds(on)} / 10\mu A$$

$$R_{ocset} = 20K, I_{oc} = 23.53A$$

$$4.5+6+5 = 15.5A \text{ max}$$

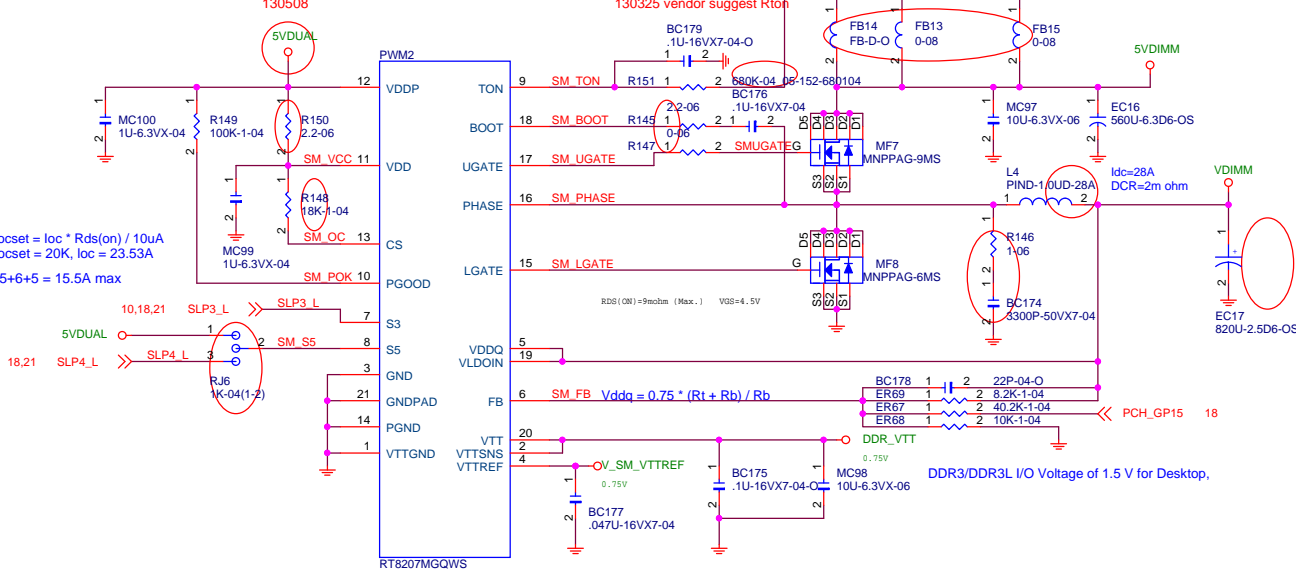


PCH DAC power

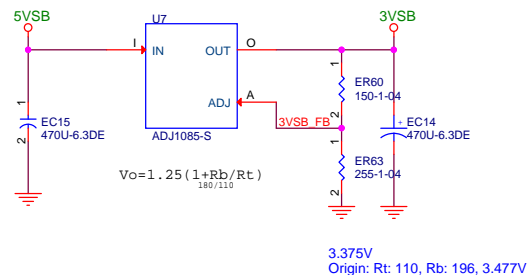
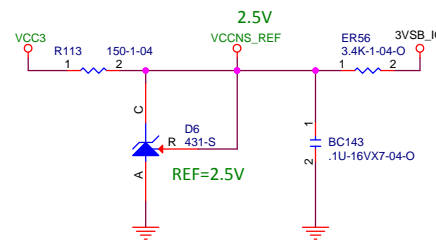


$$f = (V_{in} - 0.5) / (3.85p * V_{in} * R_{ton})$$

$$R_{ton} = 680K, f = 344K$$



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Discharge Selection for RT8207M

| TON pin connect Rton to | Discharge Mode |
|-------------------------|------------------------|
| Vin | Non-Tracking Discharge |

S3 and S5 Truth Table

| STATE | S3 | S5 | VDDQ | VTTREF | VTT |
|---------|----|----|-----------|-----------|-----------|
| S0 | H | H | OUTPUT | OUTPUT | OUTPUT |
| S3 | L | H | OUTPUT | OUTPUT | HIGH-Z |
| S4 / S5 | L | L | DISCHARGE | DISCHARGE | DISCHARGE |

FB and output voltage setting

| FB | VDDQ(V) | VTTREF and VTT | NOTE |
|--------------|------------|----------------|------------------|
| VDD | 1.8 | Vvddq/2 | DDR2 |
| GND | 1.5 | Vvddq/2 | DDR3 |
| FB Resistors | Adjustable | Vvddq/2 | 0.75V<Vvddq<3.3V |

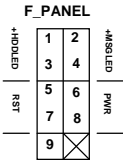
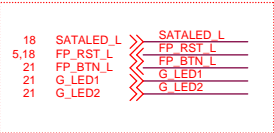


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| DC/DC PCH/DRAM | | | |
|----------------|----------------------------|-------|----------|
| Size | Document Number | Rev | |
| Custom | H81H3-I | 1.0 | |
| Date: | Wednesday, August 14, 2013 | Sheet | 11 of 27 |

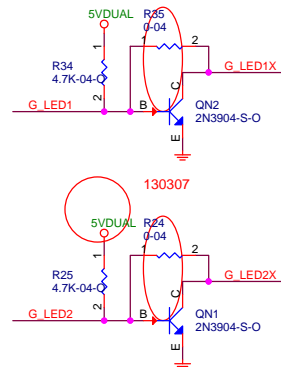
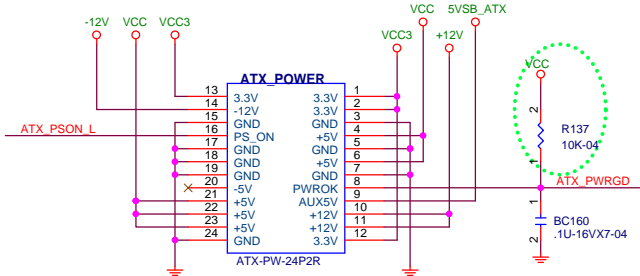
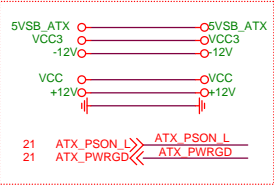
FRONT PANEL

External Connection



POWER CONNECTOR

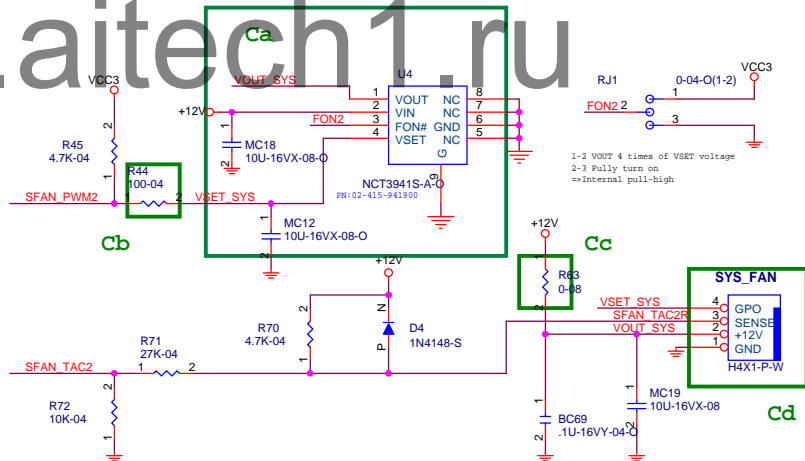
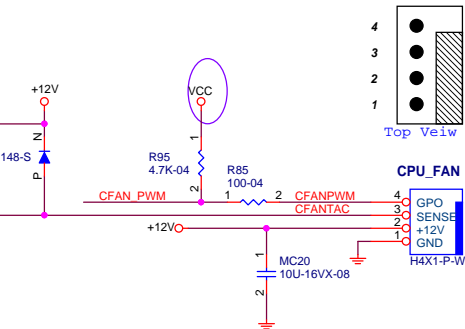
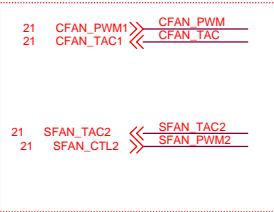
External Connection



| | | | | | |
|------|--------|----|----|----|----------|
| GP22 | G_LED1 | S0 | S1 | S3 | S4/S5 |
| GP23 | G_LED2 | H | H | L | L |
| | | G | GB | YB | OFF |
| | | | | | Blinking |

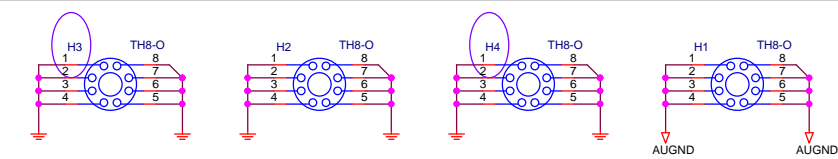
FAN

External Connection



BOM Difference

| | SYS_FAN 3PIN | SYS_FAN 4PIN |
|----|--------------|--------------|
| Ca | V | X |
| Cb | 15k | 100 |
| Cc | X | V |
| Cd | H3X1-P-W | H4X1-P-W |



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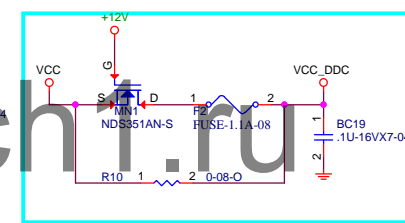
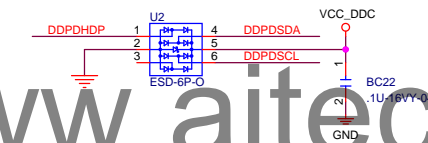
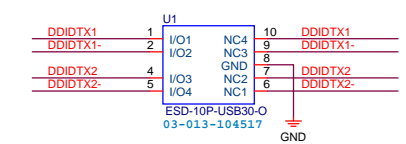
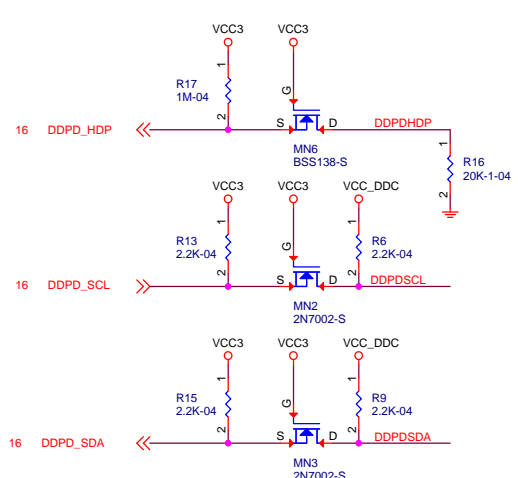
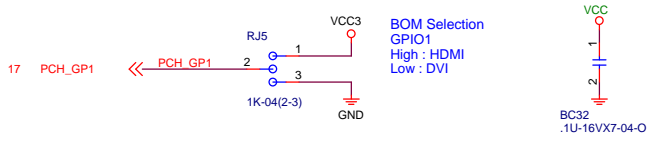
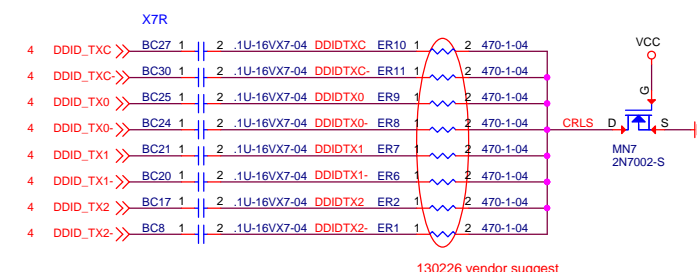
F_Panel/FAN/PWR Conn

H81H3-I

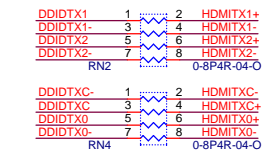
1.0

Wednesday, August 14, 2013

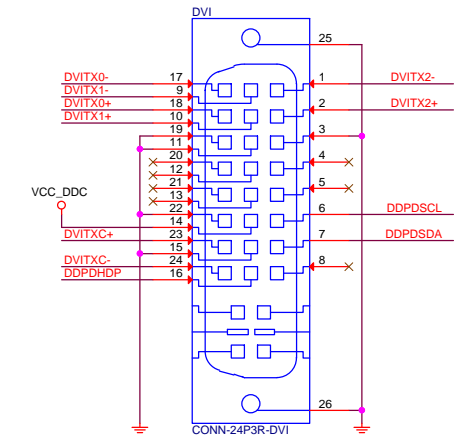
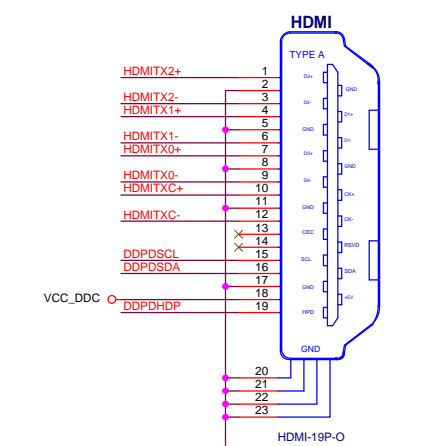
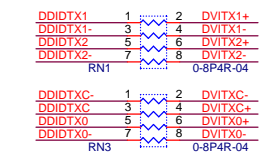
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HDMI

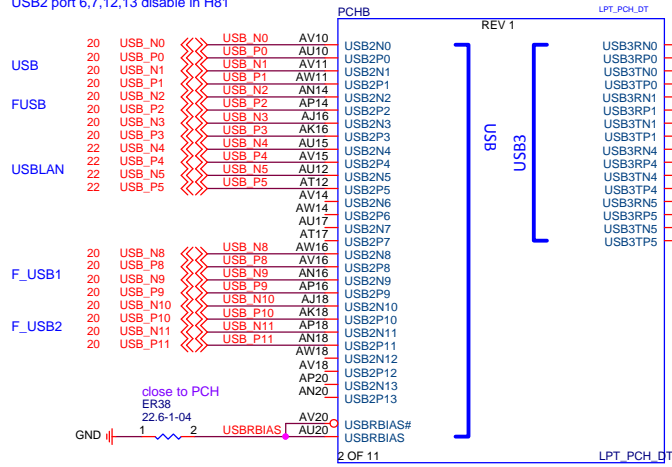


DVI



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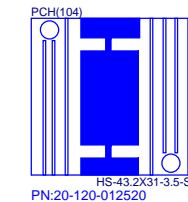
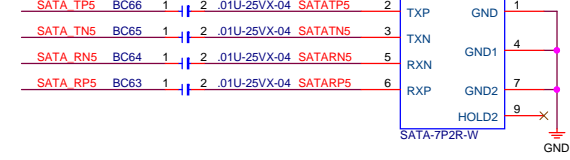
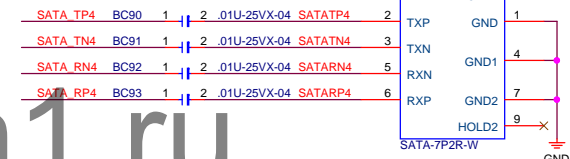
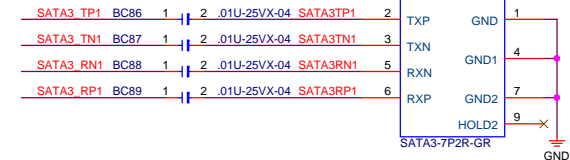
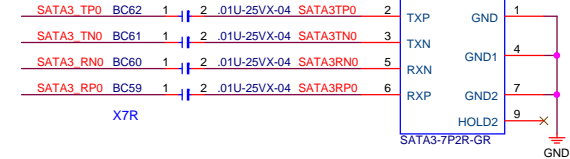
USB2 port 6,7 disable in B85
USB2 port 6,7,12,13 disable in H81



USB3 (PET port 1,2) disable in B85/H81
USB3 port 4,5 disable in H81

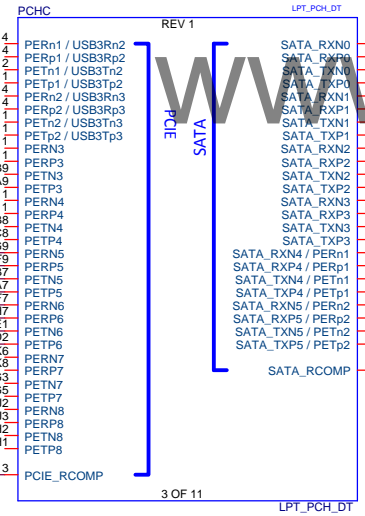
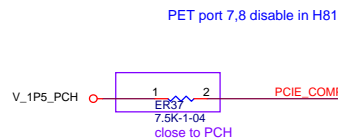
REAR USB3

SATA 6G



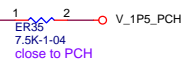
PCIEX1

LAN



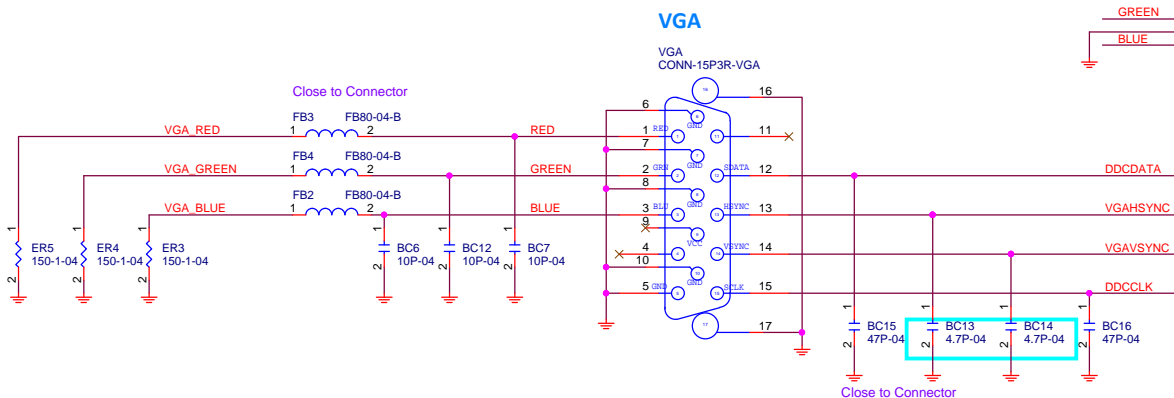
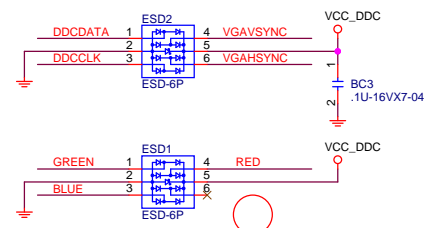
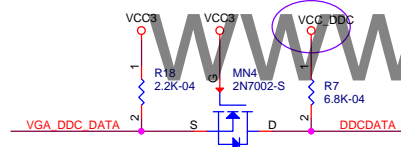
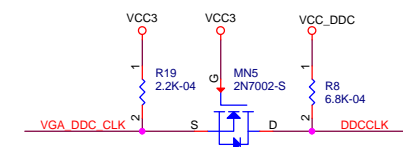
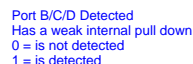
port 2,3 disable in H81
port 4,5 are SATA 3Gb/s in B85/H81

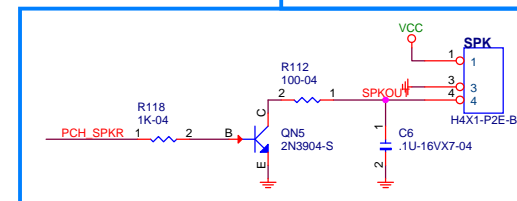
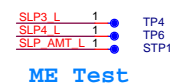
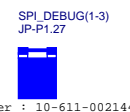
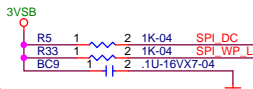
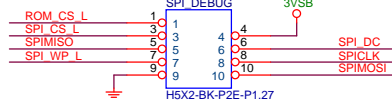
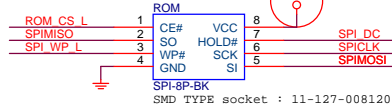
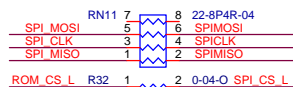
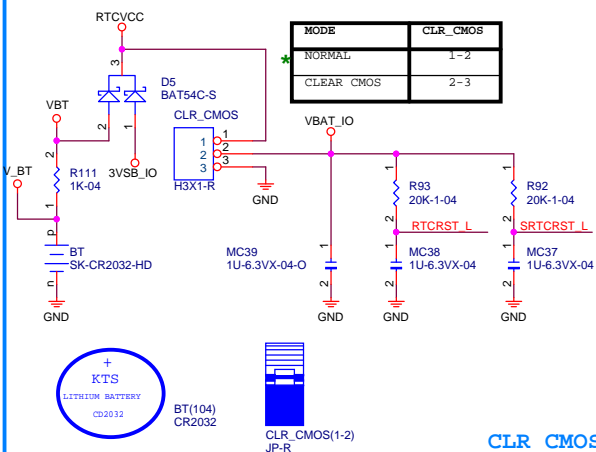
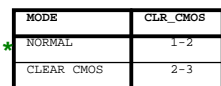
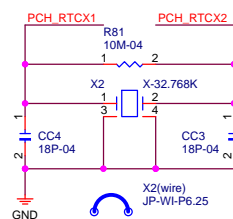
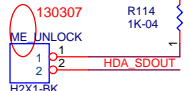
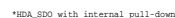
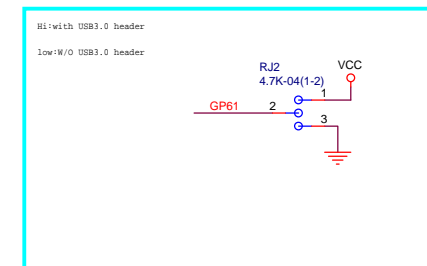
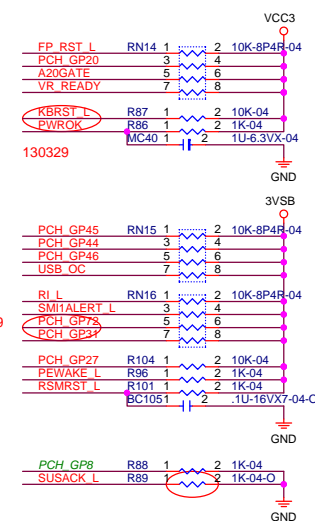
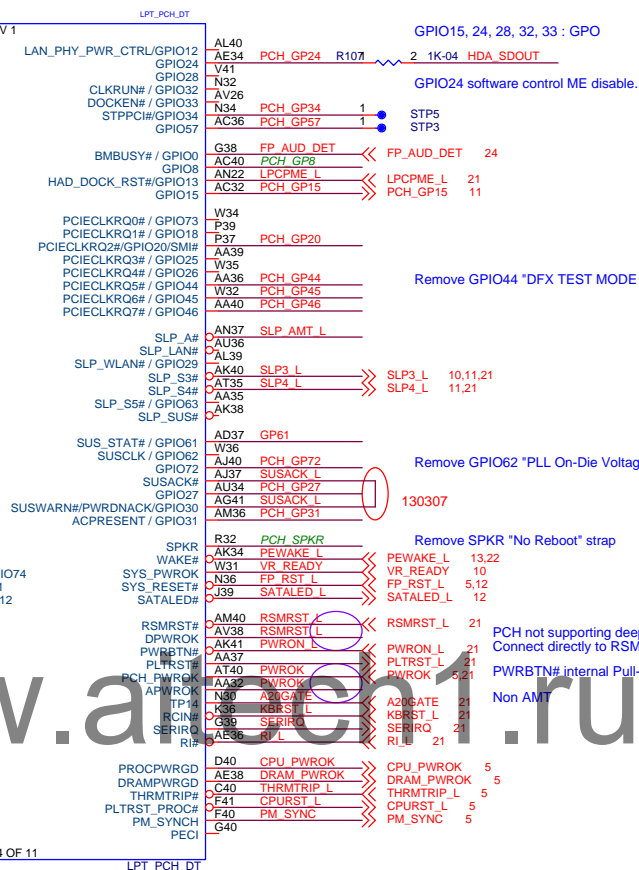
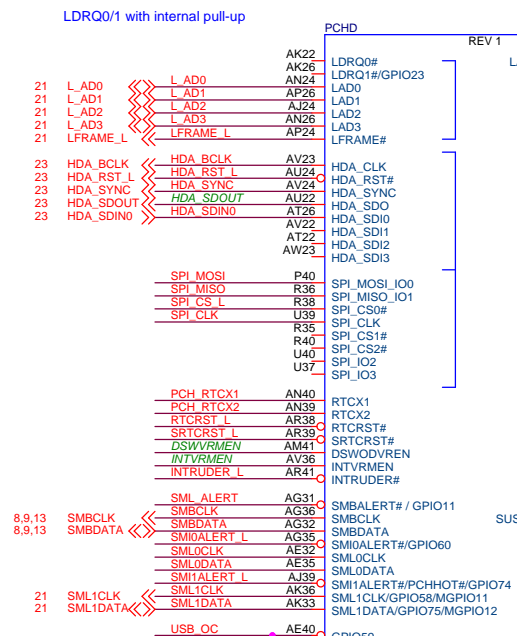
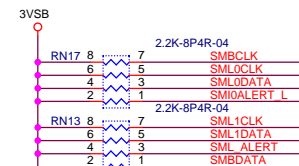
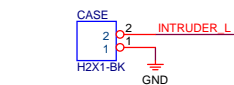
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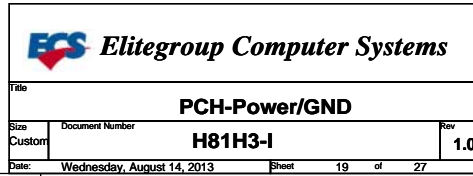


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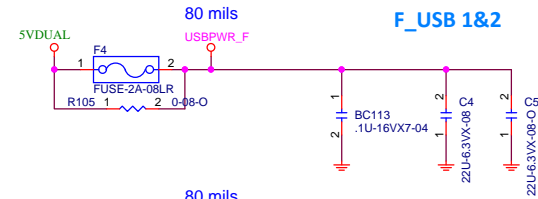
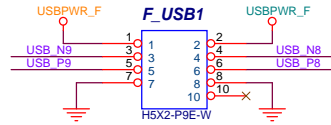
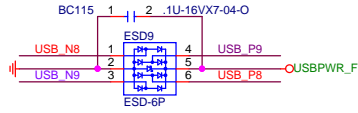
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| Title | | PCH-USB/PE/SATA | |
| Size | Document Number | H81H3-I | |
| Custom | | Rev 1.0 | |
| Date: | Monday, August 19, 2013 | Sheet | 15 of 27 |



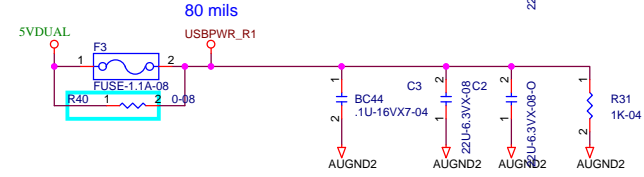
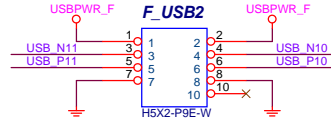
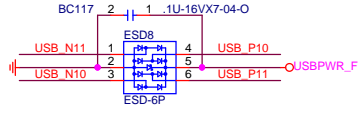




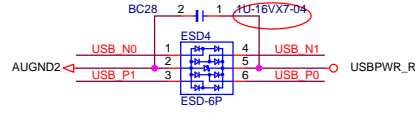
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15 USB_N8 <-> USB_N8
15 USB_P9 <-> USB_P9
15 USB_N9 <-> USB_N9



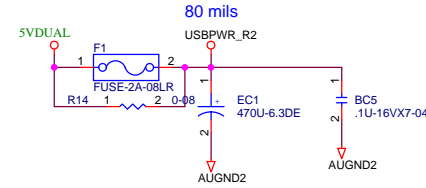
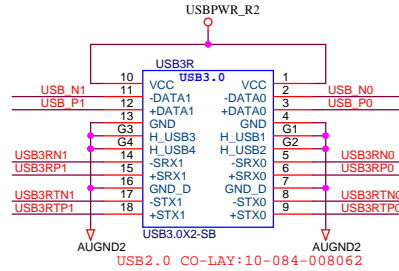
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15 USB_P11 <-> USB_P11
15 USB_N11 <-> USB_N11



15 USB_P0 <-> USB_P0
15 USB_N0 <-> USB_N0
15 USB_P1 <-> USB_P1
15 USB_N1 <-> USB_N1



USB3.0 Connector



15 USB3_TP0 <-> USB3_TP0
15 USB3_TN0 <-> USB3_TN0
15 USB3_RP0 <-> USB3_RP0
15 USB3_RN0 <-> USB3_RN0

USB3_TP0 BC33 1 2 .1U-16VX7-04 USB3TP0
USB3_TN0 BC38 1 2 .1U-16VX7-04 USB3TN0
USB3_TP1 BC29 1 2 .1U-16VX7-04 USB3TP1
USB3_TN1 BC31 1 2 .1U-16VX7-04 USB3TN1

USB2.0 CO-LAY:10-084-008062

USB3TN0 1 2 USB3RTN0
USB3TP0 3 4 USB3RTP0
USB3TN1 5 6 USB3RTN1
USB3TP1 7 8 USB3RTP1

Rear USB3.0

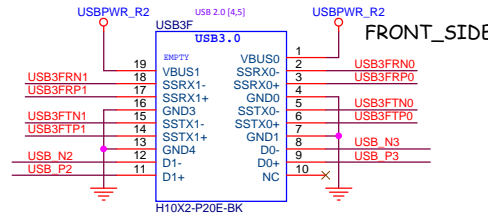
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USB3_RP0 3 4 USB3_RP0
USB3_RN1 5 6 USB3_RN1
USB3_RP1 7 8 USB3_RP1

15 USB_N2 <-> USB_P2
15 USB_P2 <-> USB_N2
15 USB_N3 <-> USB_P3
15 USB_P3 <-> USB_N3

USB3TP1 1 2 USB3FTP1
USB3TN1 3 4 USB3FTN1
USB3TP0 5 6 USB3FTP0
USB3TN0 7 8 USB3FTN0

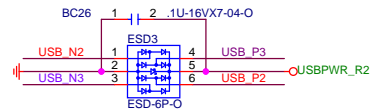
Front USB3.0

USB3_RP1 1 2 USB3FRP1
USB3_RN1 3 4 USB3FRN1
USB3_RP0 5 6 USB3FRP0
USB3_RN0 7 8 USB3FRN0



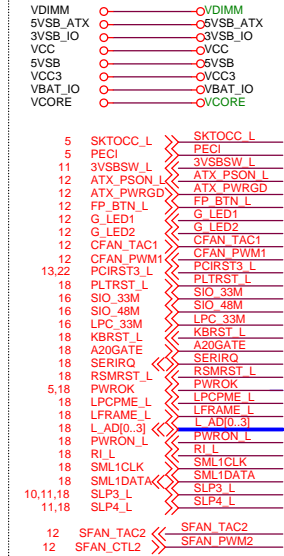
USB3_RN0 1 S1_A S1_B 10 USB3_RN0
USB3_RP0 2 S2_A S2_B 9 USB3_RP0
USB3_RN1 4 S3_A S3_B 7 USB3_RN1
USB3_RP1 5 S4_A S4_D 6 USB3_RP1

USB3TP1 1 S1_A S1_B 10 USB3TP1
USB3TN1 2 S2_A S2_B 9 USB3TN1
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USB3TN0 5 S4_A S4_D 6 USB3TN0

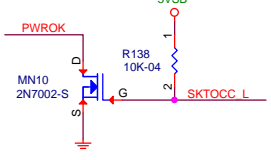
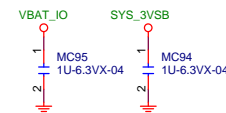
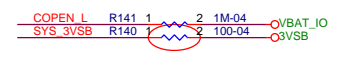
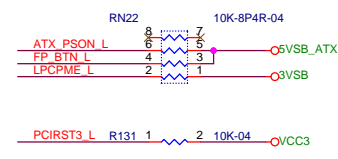
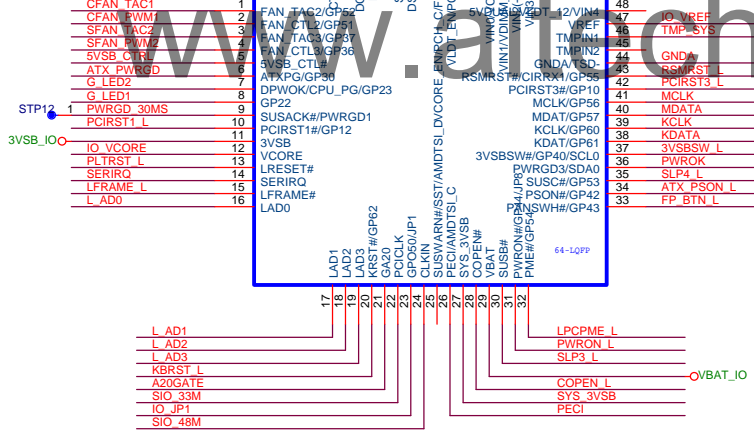
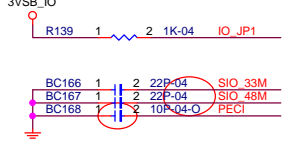
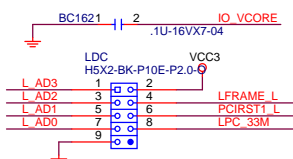
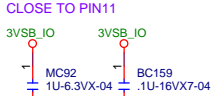
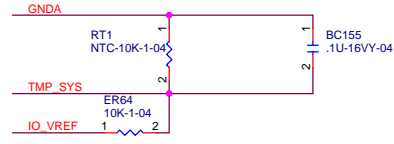
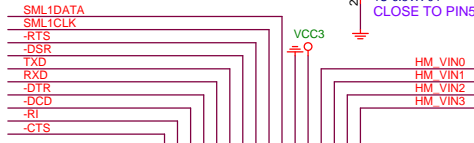
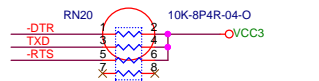
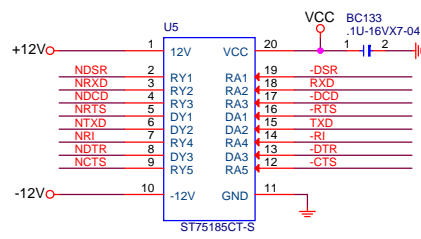
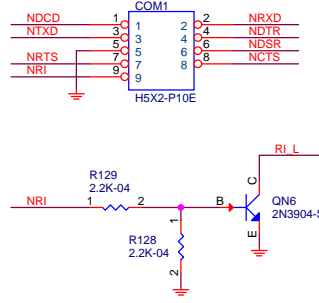


Elitegroup Computer Systems

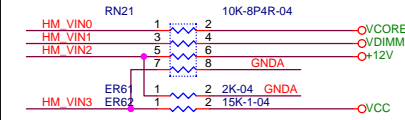
External Connection



COM Header

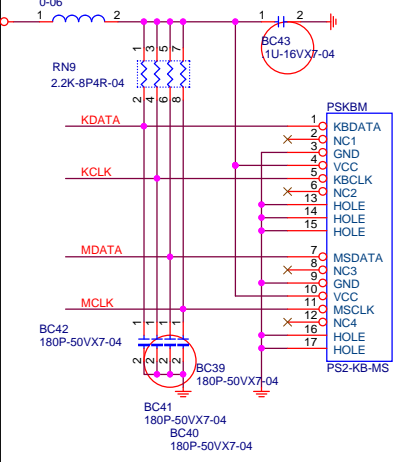


Voltage Monitor

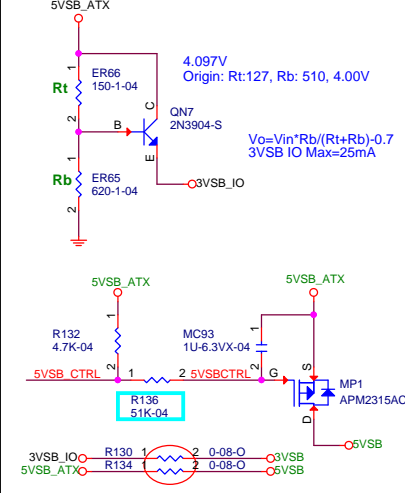


* HM_VIN0 for VCORE
* HM_VIN1 for V_DIMM

PS2



ErP



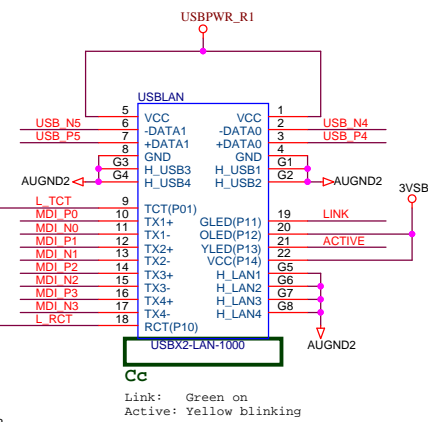
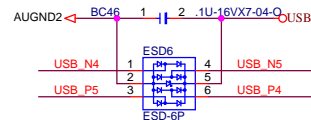
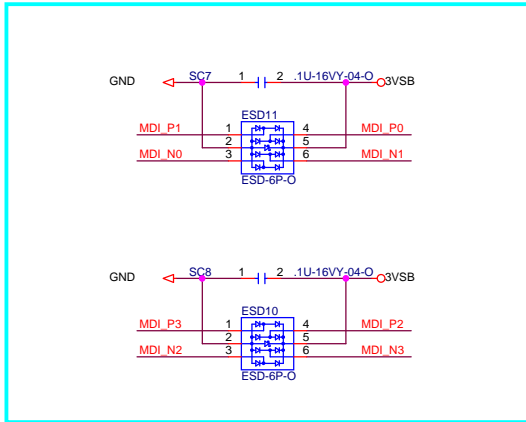
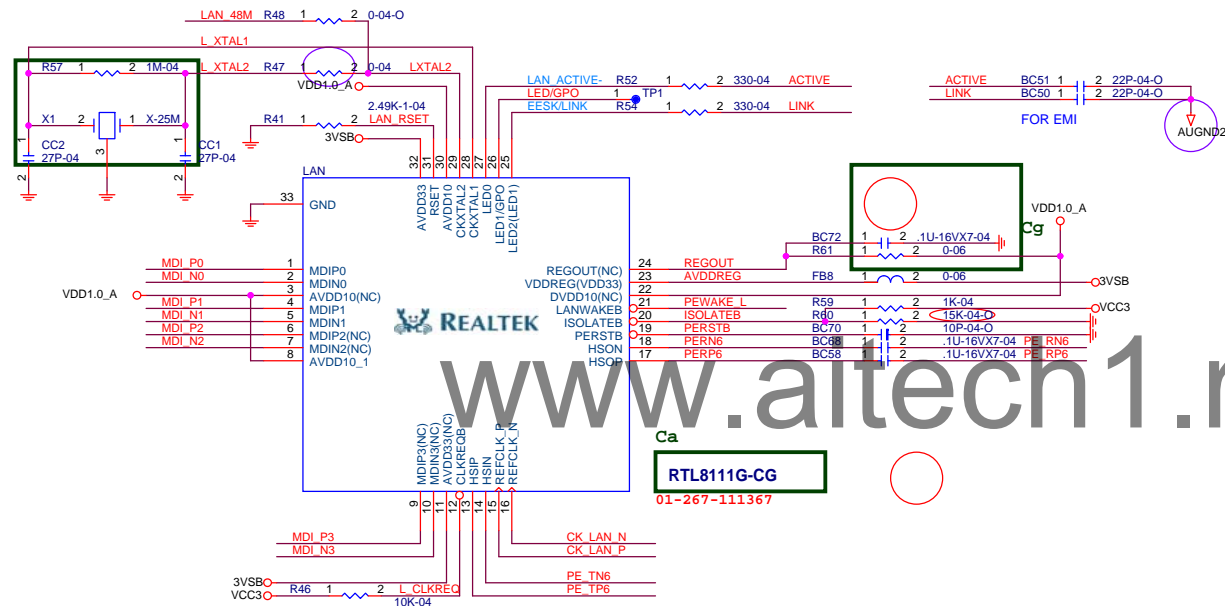
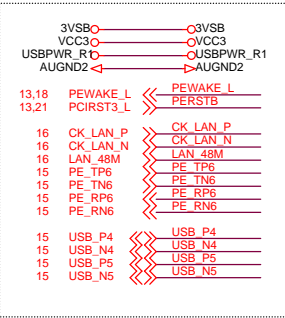
Elitegroup Computer Systems

| File | Document Number | Rev |
|------------|----------------------------|----------------|
| SIO-IT8772 | H81H3-I | 1.0 |
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IT8772 Power-On Strapping Options

| Symbol | Value | Description |
|--------|-------------------------------------|---------------------------------------|
| JP1 | DSW_EUP_SEL | 1 EUP(default) |
| JP2 | WDT_EN | 0 Disable WDT to reset PWROK(default) |
| Pin-57 | Enable WDT to reset PWROK | 1 Enable WDT to reset PWROK |
| JP3 | FAN_CTL_SEL | 1 EC Index 6Bh/73h default = 80h |
| Pin-59 | EC Index 6Bh/73h default = 00h | 0 EC Index 6Bh/73h default = 00h |
| JP4 | K8PWR_EN | 1 Disable K8 Power Sequence(default) |
| Pin-61 | Enable K8 Power Sequence | 0 Enable K8 Power Sequence |
| JP8 | RSMRST_SEL | 1 RSMRST# output detected by 3VSB |
| Pin-31 | RSMRST# output detected by SYS_3VSB | 0 RSMRST# output detected by SYS_3VSB |

External Connection



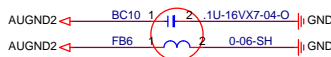
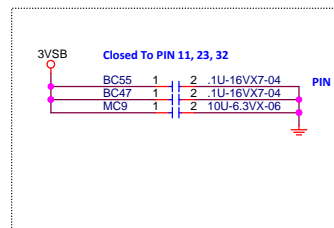
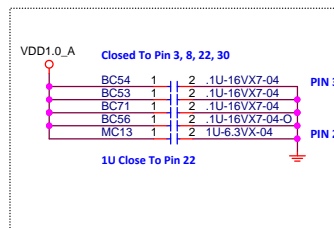
BOM Difference

DEFAULT

| | RTL8111G-CG (LDO mode) | RTL8106E-CG (LDO mode) |
|----|---------------------------|---------------------------|
| Ca | RTL8111G-CG | RTL8106E-CG |
| Cc | USBX2-LAN-1000 | USBX2-LAN-100 |
| Cd | X | V |
| Ce | 0-04 | .01U-25VX-04 |
| Cg | R | X |

8106E : NC PIN - 3,6,7,9,10,11,22,24

MC15,BC46,BC35 -O,BC41 1U-6.3VX-04

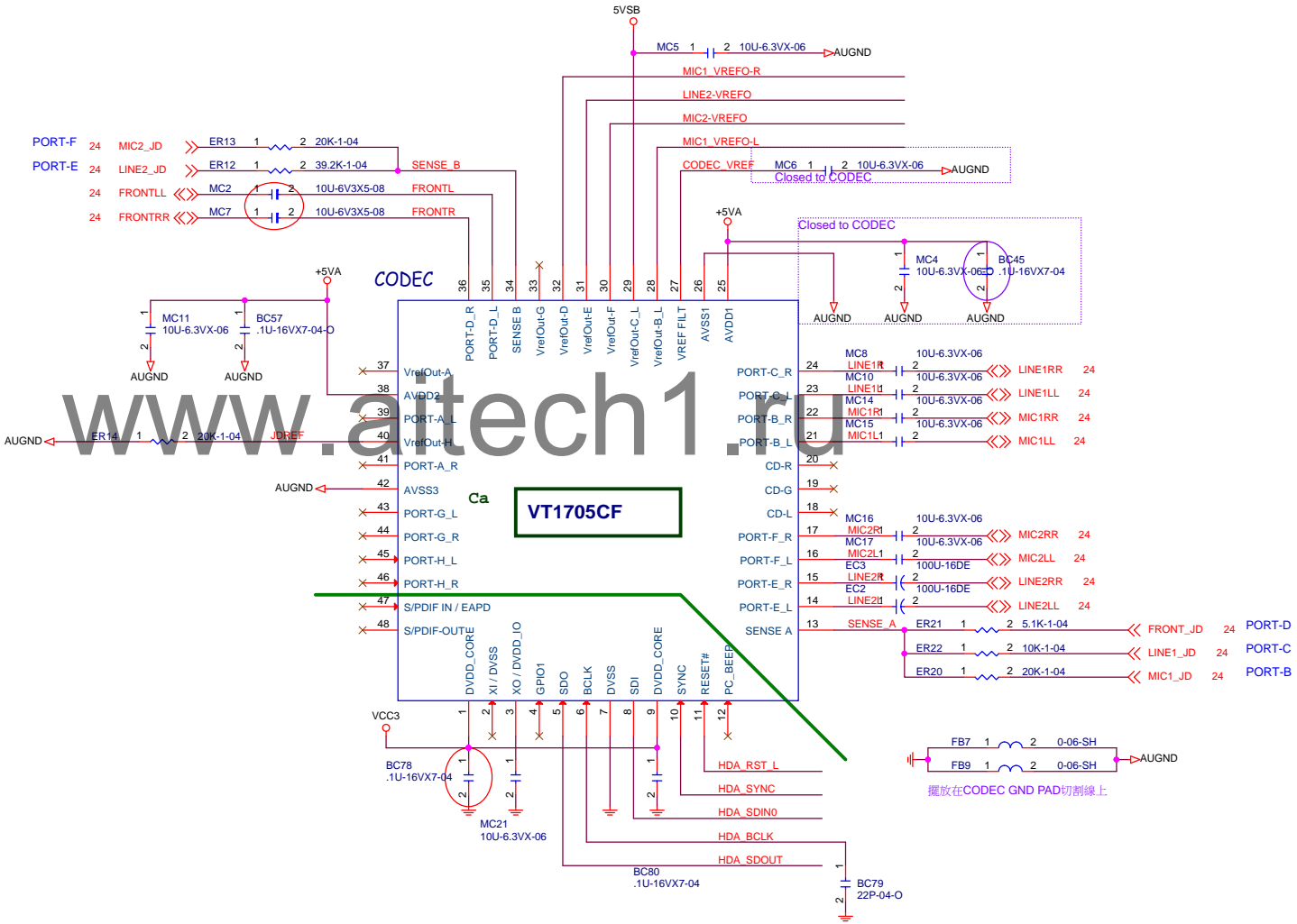
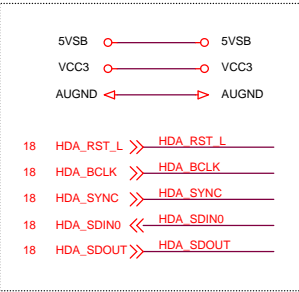


LAN-RT8111GS/8106E

H81H3-I

1.0

External Connection



Pin Difference

| Pin | ALC662VD | VT1705CF |
|-----|--------------|------------------------------|
| 2 | GPI00 | GPI00/SPDIF_TX1/ DMIC_CLK |
| 3 | REG VREF | REGREF |
| 4 | GPI01 | GPI01/DMIC_DATA |
| 25 | LDO OUTPUT | LDO_OUT1 |
| 29 | LDO VIN | LDO_IN |
| 33 | LINE1 VREF | SENSE_C |
| 37 | FRONT VREF ? | VREFOUT_C |
| 38 | LDO OUTPUT | LDO_OUT2 |
| 45 | DMIC DATA | NC |
| 46 | DMIC CLK | NC |
| 47 | EADP | EADP/SPIDF_RX |

01-278-662350 02-301-705622

BOM Difference

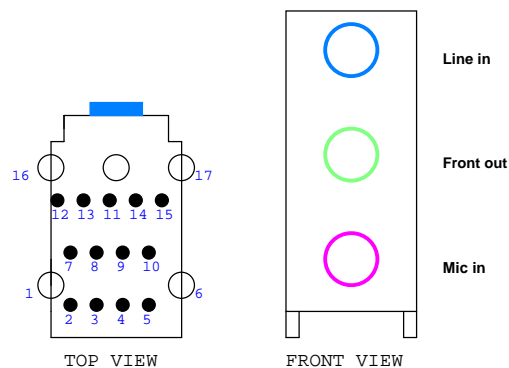
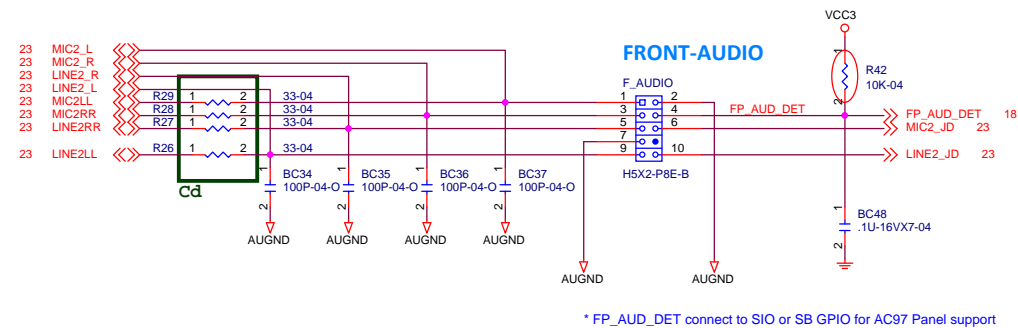
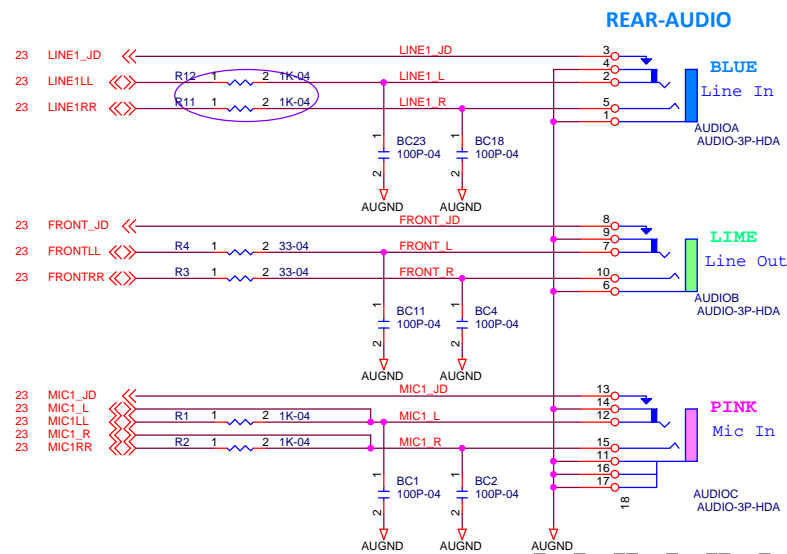
| Location | ALC662VD | VT1705CF |
|----------|---------------|----------|
| Ca | ALC662-VD0-GR | VT1705CF |
| Cb | V | X |
| Cc | 2.2K-04 | 3.3K-04 |
| Cd | 75-04 | 33-04 |

When you change BOM, remember change GPL to inform BIOS use different VerB-Table.

VT1705CF(Chip)

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